WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

subword drivers (SWDs), each of which has a plurality of subword driver circuits commonly connected to a main word line and also connected to different subword selection lines to drive respective subword lines, each of the SWDs being connected to driver input terminals and the subword lines; and

a common inverter circuit having an inverter input terminal and an inverter output terminal, the inverter input terminal being connected to the main word line and the inverter output terminal being connected to the plurality of driver input terminals,

wherein each of the subword driver circuits includes an internal inverter circuit that is connected to an inverter output terminal connected to the main word line and the subword selection lines and has its output terminal connected to the subword lines, and a drive transistor connected to the subword selection lines, the inverter output terminal and the output terminal of the internal inverter circuit, and

each of the subword driver circuits is driven by a subword selection signal received through one of the subword selection lines.

2. The semiconductor memory device according to Claim 1, wherein

the internal inverter circuit is constructed of a PMOS transistor and an NMOS transistor having their gates and drains commonly connected to the main word line, and

the source of the PMOS transistor is structured to the subword selection lines, and an output of the internal inverter is taken out from the commonly connected drains.

3. The semiconductor memory device according to Claim 2, wherein the drive transistor is structured by an NMOS transistor having a drain connected to the subword selection lines, a source connected to the subword

lines, and a gate connected to the output terminal of the common inverter circuit.

4. The semiconductor memory device according to Claim 1, wherein the common inverter circuit is structured by two transistors.

5. The semiconductor memory device according to Claim 4, wherein the common inverter circuit and the main word line are shared by four subword driver circuits.

6. A subword driver driving system for driving a plurality of subword drivers (SWDs), which are disposed on branched subword selection lines, by issuing subword selection signals represented by FXB(/FX),

wherein a plurality of inverters is connected at the branching positions on the subword selection lines to turn the subword selection signals into true subword selection signals expressed by FXT and distribute the true subword selection signals to the plurality of SWDs provided at the branching positions of the subword lines so as to reduce the load applied to the FXB subword selection signals.

7. The subword driver driving system according to Claim 6, wherein

the SWDs are disposed on both sides with the subword selection lines sandwiched therebetween, and

the SWDs on both sides receive the true subword selection signals from the inverters shared by them.

8. The subword driver driving system according to Claim 7, wherein

the SWD comprises an inverter having its inverter input terminal connected to a main word line and an inverter output terminal thereof connected to the SWD, and subword driver circuit that is connected to the inverter output terminal and receives the true subword selection signals,

wherein the subword driver circuit is connected to the inverter input terminal connected to the main word line and comprises an internal inverter circuit that is connected to subword selection lines for receiving the true subword selection signals and has its output terminal connected to the subword

lines, and a drive transistor connected to the subword selections lines to which the true subword selection signals are supplied, the inverter output terminal, and the output terminal of the internal inverter circuit, and

the subword driver circuit is driven by the true subword selection signals.